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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,353	10/18/2000	James W. Adkisson	BUR9-1999-0300-US1	3972

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,353	ADKISSON ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 14-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 14-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *06/02/05* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The non-final rejection as set forth in paper No. (031605) mailed on March 18th, 2005 is withdrawn in response to applicants' argument in the telephonic interview on June 02nd, 2005. A new rejection is made as set forth in this Office Action. Claims (1 and 14-30) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 14-30 are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated by Adkisson et al. (U.S. Patent 6,563,131).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 1, **Adkisson** discloses a method of forming a field effect transistor (FET) transistor, comprising: providing a substrate **10**; forming a layer on the substrate **10**, the layer having exposed vertical side surfaces on opposite sides of the layer, the

layer being able to support epitaxial growth on the side surfaces (col. 3, lines 3-25 and FIG. 1B);

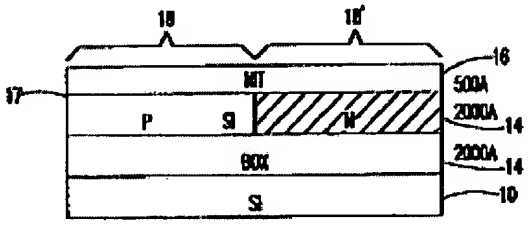

FIG. 1B

forming an epitaxial channel **Si** on the each of the exposed side surfaces of the layer, the channel having an exposed first sidewall opposite the vertical side surface of the layer (FIG. 1C);

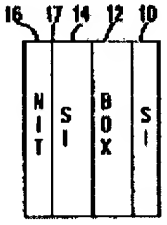

FIG. 1C

removing a channel on a first vertical side surface of the layer and then removing the layer, thereby exposing a second vertical sidewall of the channel formed on the second vertical side of the layer (col. 4, lines 9-24 and FIG. 10C);

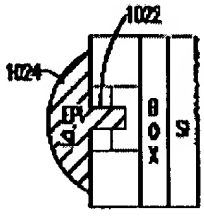

FIG. 10C

forming a second channel **1024** in place of removed channel; and forming a gate **G** adjacent to at least one of the sidewalls of the channel and the second channel **SI**, there being a gate dielectric **1022** between each channel **SI** and the gate **G** (FIG. 11D).

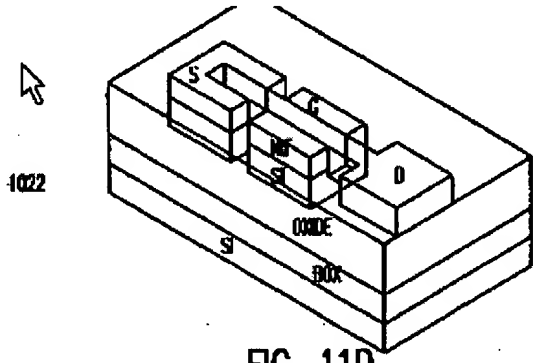

FIG. 11D

In re claim 14, **Adkisson** discloses a method for forming a double gated field effect transistor (FET), comprising the steps of: forming on a substrate a first and second epitaxially grown channels, the channels having vertical side surfaces extending up from the substrate (col. 3, lines 3-59 and FIGS. 11B-C),

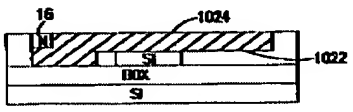

FIG. 11B

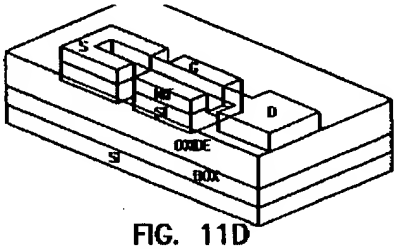

FIG. 11D

wherein the second channel **1024** is grown following removal of a central semiconductor region centered between the channels upon one of whose opposite vertical sides the first channel was grown (col. 5, line 60 to col. 5, line 9 and FIG. 10C);

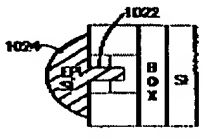

FIG. 10C

etching areas within a silicon layer to form a source **S** and a drain **D**, wherein a side surfaces of the source and the drain contact opposing end surfaces of the first and second epitaxially grown channels Si (FIG. 11D); and

forming a gate **G** that contacts a top surface and two side surfaces of the first and second epitaxially grown channels **SI** and a top surface of the substrate (FIGS. 11B-D).

In re claim 15, **Adkisson** discloses that the forming step comprises the steps of: forming first and second semiconductor lines, each end of the silicon lines contacting one of the source **S** and the drain **D**; forming an etch stop layer **12** on an exposed side surface of each of the first and second semiconductor lines (col. 3, lines 4-47 and FIG. 1B);

epitaxially growing first and second semiconductor layers **SI** on each etch stop layer **12** (FIGS. 1B-C);

etching away the first and second semiconductor lines and the etch stop layers (col. 4, lines 9-24);

filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source and the drain with an oxide fill (col. 3, line 60 to col. 4, line 8 and FIG. 3B); and

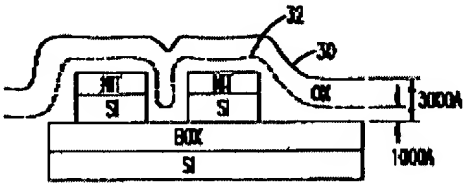

FIG. 3B

etching a portion of the oxide fill **30** to form an area that defines a gate **G**, wherein the area that defines the gate is substantially centered between and substantially parallel to the source **S** and the drain **D** (FIG. 11D);

In re claim 16, **Adkisson** discloses that the method as recited in claim 15, further comprising the steps of: etching the oxide fill between the gate **G** the source **S** to expose the first and second epitaxially grown silicon layers; and etching the oxide fill between the gate **G** and the drain **D** to expose the first and second epitaxially grown silicon layers (col. 3, line 60 to col. 4, line 24 and FIG. 11D).

In re claim 17, **Adkisson** discloses that the method as recited in claim 16, further comprising the step of forming an oxide **30** on the first and second epitaxially grown silicon layers (FIG. 3B).

In re claim 18, **Adkisson** discloses that the oxide is silicon dioxide (col. 3, line 60 to col. 4, line 8).

In re claim 19, **Adkisson** discloses that the method as recited in claim 14, further comprising the steps of: implanting a portion of the epitaxially grown silicon layers **SI** between the gate **G** and the source **S**; and implanting a portion of the epitaxially grown silicon layers between the gate **G** and the drain **D** (FIG. 11D).

In re claim 20, **Adkisson** discloses that the implanting step is in the range of 10 to 45 degrees relative to a vector perpendicular to a top surface of the epitaxially grown silicon layers (FIG. 11D).

In re claim 21, **Adkisson** discloses that the implants are done in a series at approximately 90 degrees relative to each other (FIG. 11D).

In re claim 22, **Adkisson** discloses that the method as recited in claim 14, further comprising the step of forming a contact **1220** on each of the gate **G**, the source **S** and the drain **D** (col. 5, line 10-22 and FIG. 12B).

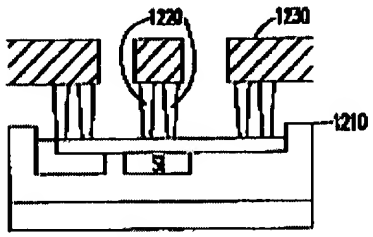

FIG. 12B

In re claim 23, **Adkisson** discloses that the method as recited in claim 14, wherein the gate material is polysilicon (col. 4, lines 35-48).

In re claim 24, **Adkisson** discloses a method of forming an FET, comprising: forming on a substrate **10** a first semiconductor layer having first and second ends and a central region that is thinner than the first and second ends, the central region having first and second side surfaces extending upward from the substrate, the semiconductor layer being able to support epitaxial growth on the first and second side surfaces (col. 4, lines 9-24 and FIG. 6B);

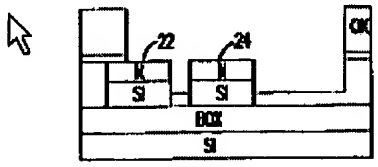

FIG. 6B

epitaxially growing a semiconductor channel region on at least one of the first and second side surfaces of the central region of the first semiconductor layer, a first side of the channel being exposed (FIG. 6B);

removing the central region of the first semiconductor layer, thereby exposing a second side of the channel; forming a dielectric layer on exposed surfaces of the semiconductor channel region; and forming a gate electrode on the dielectric layer (FIG. 11D).

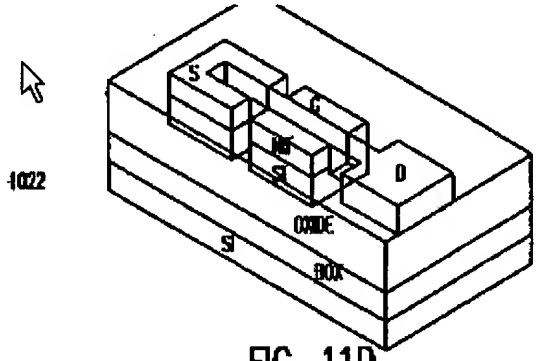

FIG. 11D

In re claims 25-27, **Adkisson** discloses where in the semiconductor channel region is formed of an alloy of silicon and a Group IV element wherein the semiconductor channel region is formed of a material selected from the group consisting of silicon, silicon-germanium, and silicon-germanium carbon (col. 3, lines 26-40).

In re claim 28, **Adkisson** discloses that the step of removing the first semiconductor layer does not appreciably remove the semiconductor channel region (col. 4, lines 9-48).

In re claim 29, **Adkisson** discloses that an etch stop is epitaxially grown between the first semiconductor layer and the semiconductor channel region (col. 3, lines 48-58).

In re claim 30, **Adkisson** discloses that the method as recited in claim 24, wherein the gate electrode is formed of a material selected from the group consisting of polysilicon, silicon-germanium, refractory metals, Ir, Al, Ru, Pt, and titanium nitride (col. 4, lines 35-48).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
September 5th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER